EE 445L Lab 7: Design and Layout of an Embedded System

Jake Desjarlais and Ashvin Roharia

10/28/16

Requirements Document

1. Overview

1.1. Objectives:

The objectives of this project is to build the noise cancelling feature for headphones. We will adjust the sound emitted by the headphones to cancel out input sound from 2 mics.

1.2. Roles and Responsibilities:

Ashvin and Jake are the engineers and the TA, Dr. Valvano, and other EE 445L students are the clients. We will divide the work of this project evenly, splitting up working on the mic, headphone, switches, and screen interface. Both students are expected to understand all aspects of the design by the end of the project.

1.3. Interactions with Existing Systems:

The system will use the TM4C123 board and a solderless breadboard. It will be powered using the USB cable.

2. Function Description

2.1. Functionality:

The system will cancel sound from a particular direction for the user. The user will be able to toggle the sound cancellation and adjust distance and output amplitude. The mic will send an analog signal to the TM4C ADC. The microcontroller will then invert the input sound and apply a very precise delay to the sound which is then sent to the speaker and headphones as output. This will result in a much lower perceived DB rating from sounds originating in the direction the microphone is oriented. We will also need to properly scale the samples taken from the microphone to compensate for any flaws in our hardware as these measurements need to be very accurate to cancel the sound properly.

2.4. Performance:

The system will operate at a frequency of 128,000 samples per second in order to keep the physical tolerances high enough that we can easily manufacture the system ourselves. This allows a high degree of software adjustability to compensate for our relatively lacking physical fabrication tolerances (ie high sample rate means we don't need to place the mic and speaker within a certain range of micrometers as we can adjust the placement with software settings). We accomplish this by optimizing the sampling interrupts to as few cycles as possible so we can set the timing offsets as accurately as possible. It is possible we may set the sample rate to even higher if we can. We will use the native 12 bit DAC and ADC on the TM4C for our conversation, which will likely be our bottleneck

2.5. Usability:

There will be 4 switch inputs one to toggle the sound cancellation and two for adjusting the speaker/microphone distance setting, and one to calibrate silence. The DAC will be interfaced to a headphone jack and an ADC will be interfaced to 2 mics. A user could use this to block traffic noise, loud classmates or noisy construction.

3. Deliverables

3.1. Reports:

The reports for Labs 7 and 11 will be written.

3.2. Outcomes:

Lab 7 Outcome:

A) Objectives
- 1-page requirements document

B) Hardware Design
- Regular circuit diagram (SCH file)
- PCB layout and three printouts (top, bottom and combined)

C) Software Design
- Include the requirements document (Preparation a)

D) Measurement Data
- Give the estimated current (Procedure d)
- Give the estimated cost (Procedure e)

Lab 11 Outcome:

A) Objectives
- 2-page requirements document

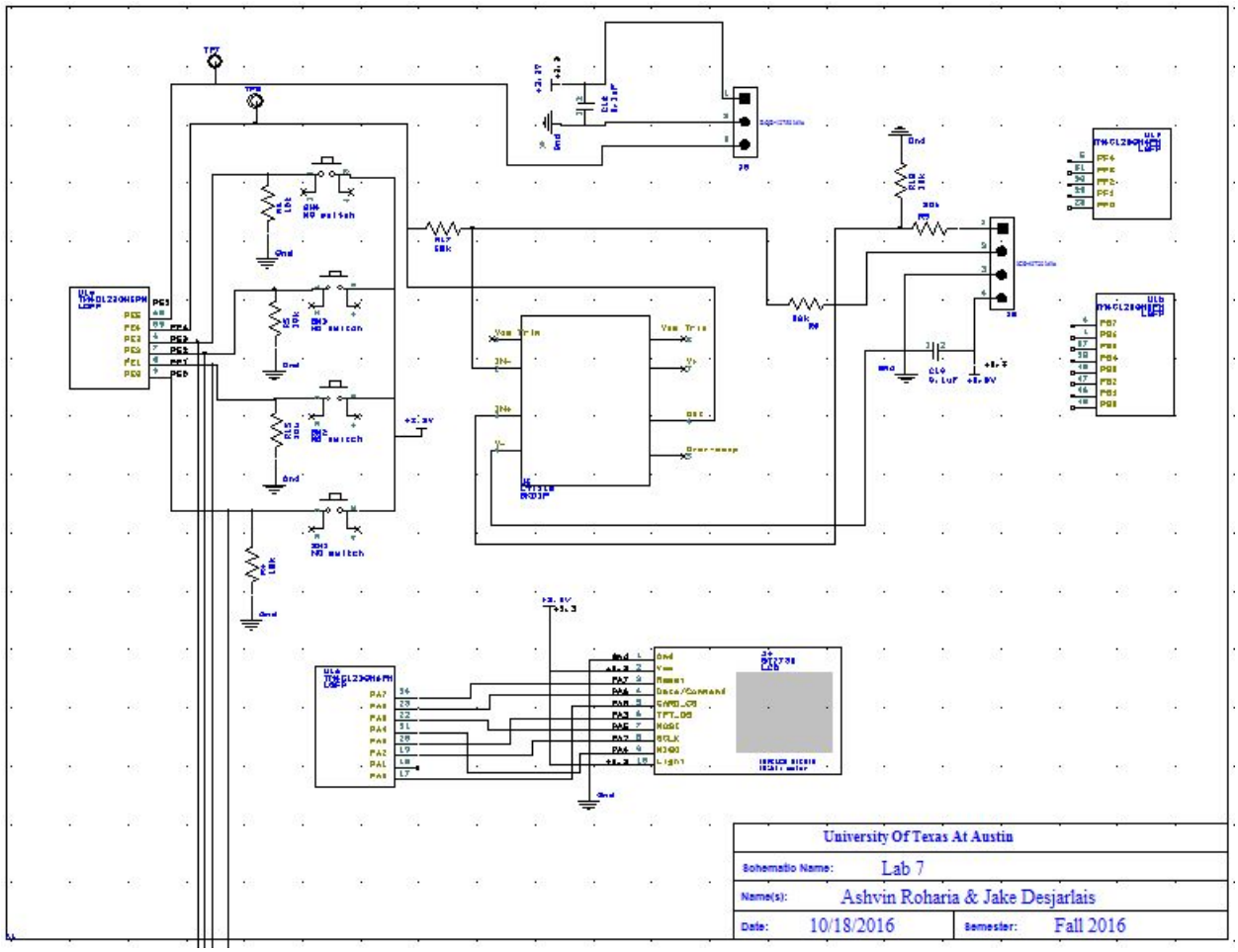
B) Hardware Design
- Detailed circuit diagram of the system (from Lab 7)

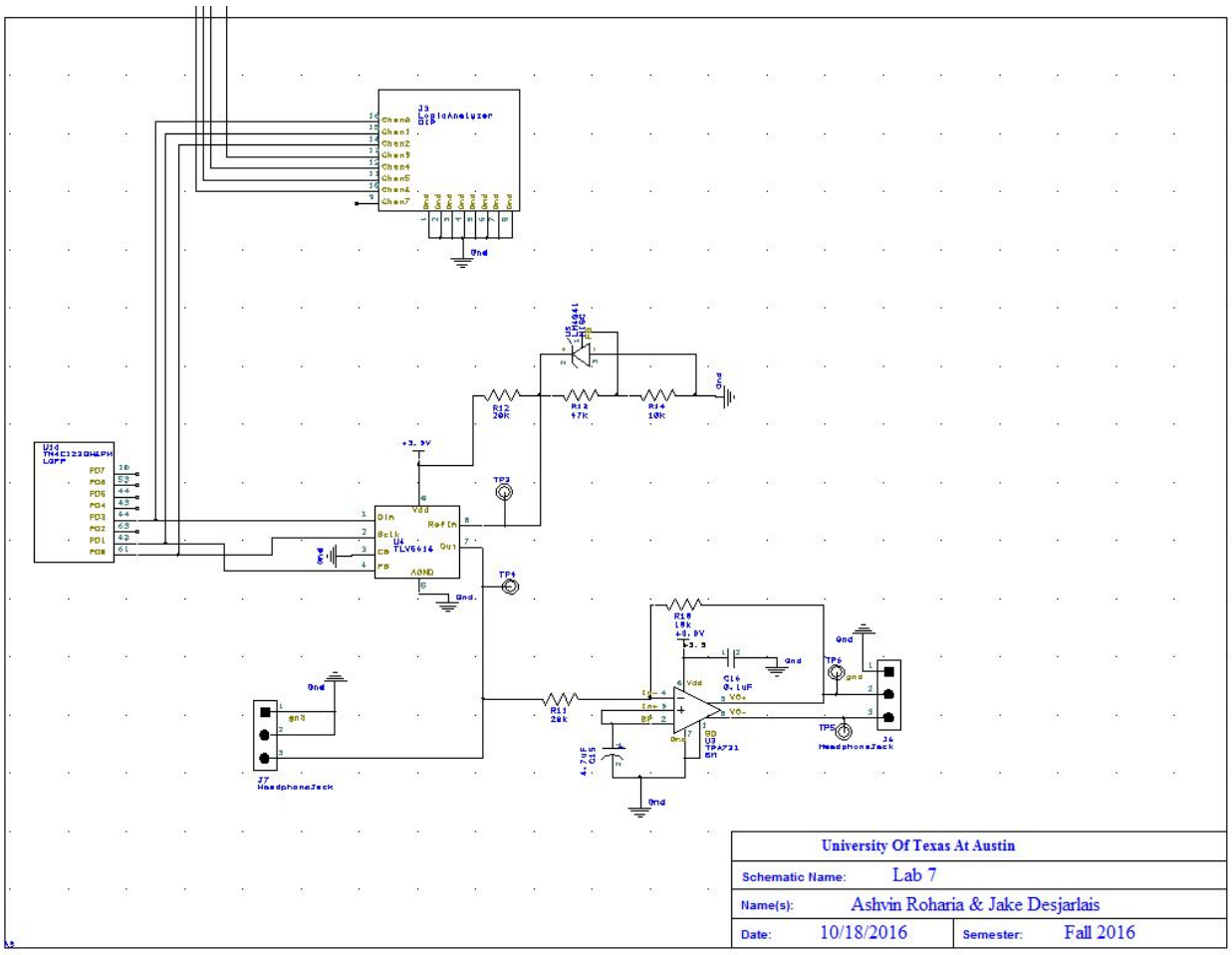
C) Software Design (no software printout in the report)
- Briefly explain how your software works (1/2 page maximum)

D) Measurement Data
- Include data as appropriate for your system. Explain how the data was collected.

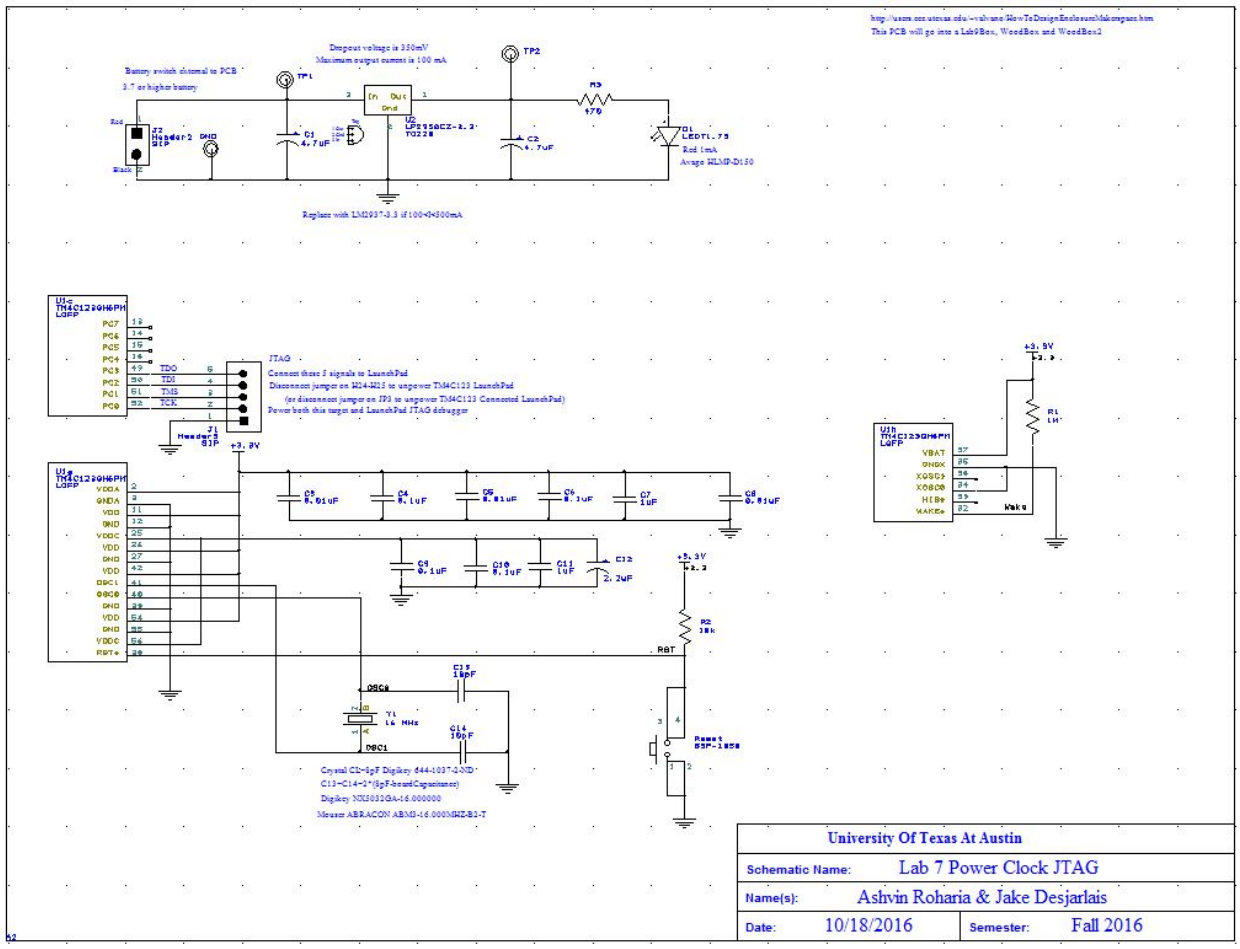
Hardware Design

Regular circuit diagram (SCH file)



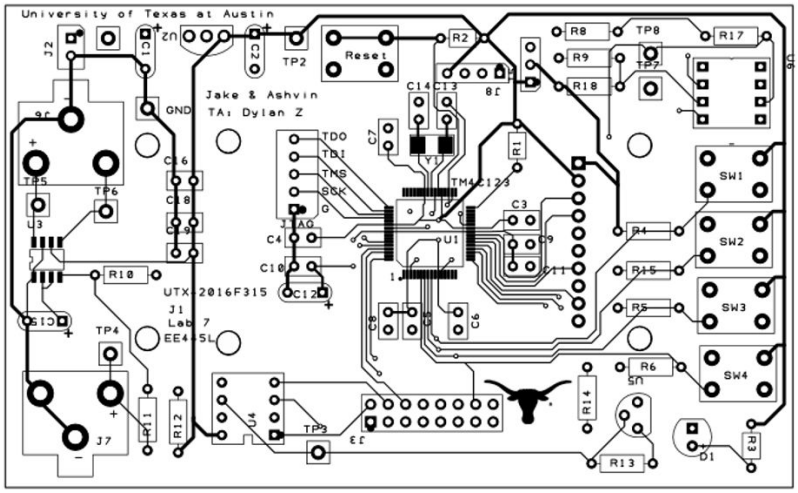


University Of Texas At Austin			
Schematic Name:	Lab 7		
Name(s):	Ashvin Roharia & Jake Desjarlais		
Date:	10/18/2016	Semester:	Fall 2016

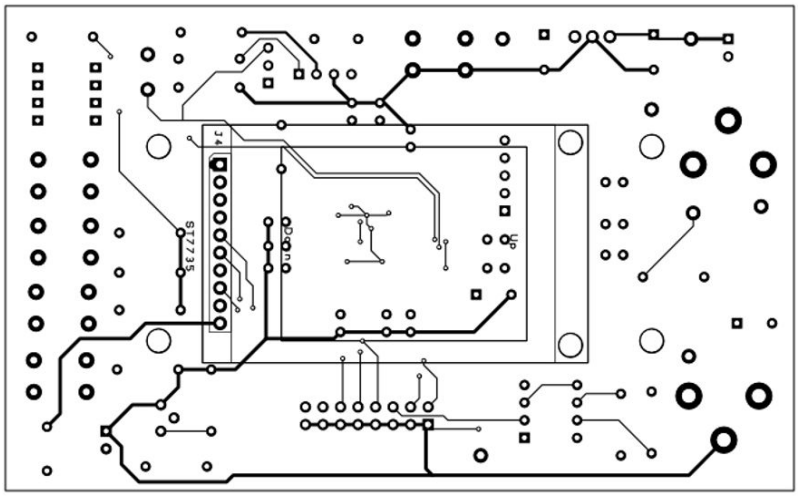


University Of Texas At Austin			
Schematic Name:	Lab 7 Power Clock JTAG		
Name(s):	Ashvin Roharia & Jake Desjarlais		
Date:	10/18/2016	Semester:	Fall 2016

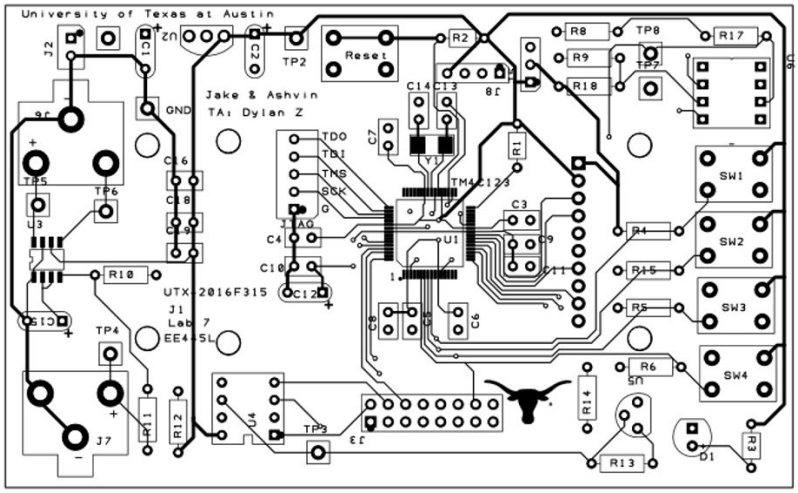
Top Silk

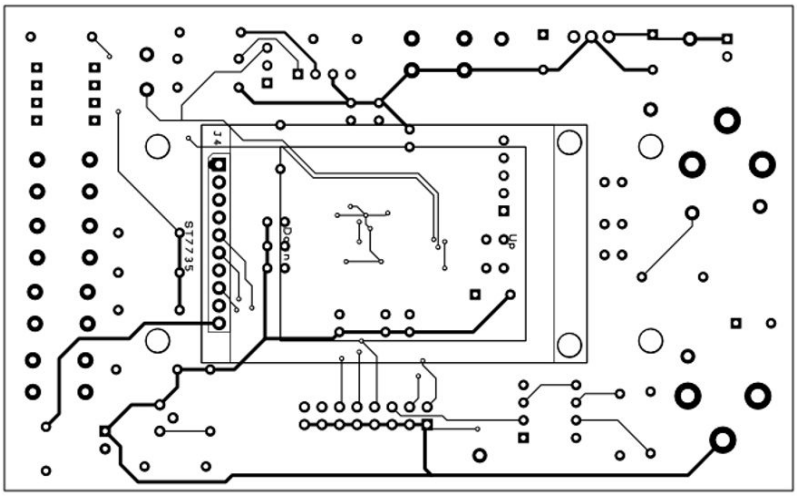

University of Texas at Austin
Jake & Ashvin
TA: Dylan Z
UTX-2016F315
J1
Lab 7
EE445L
Reset
TP2
GND
TDO
TDI
TMS
SCK
JTAG
TM4C123
U1
SW1
SW2
SW3
SW4
TP8
TP7
R8
R9
R18
R17
R2
R1
R4
R15
R5
R6
R10
R11
R12
R13
R14
R3
D1
TP4
TP5
TP6
TP3
J2
J3
J4
J7
J8
U2
U3
U5
U6
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C18
Y1

Bottom Silk



Top and Bottom Silk





Measurement Data

Give the estimated current

The estimated currently supply current is 75mAh.

Give the estimated cost

The estimated total cost is $66.51. The estimated out-of-pocket cost is $27.21.